WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

conductive patterns formed on a semiconductor substrate;

dielectric patterns disposed between the conductive patterns on the substrate, each having a cross-section with an upside-down T shape and having greater thickness than the conductive patterns;

a nitride film liner lining trenches defined by the conductive patterns and the dielectric patterns;

a dielectric layer on the nitride film liner, filling the trenches; and

at least one metal contact plug passing through the dielectric layer and the nitride film liner and in contact with at least one of the conductive patterns.

2. The integrated circuit of Claim 1, further comprising:

first and second gates and first and second sources/drains;

a lower dielectric layer formed on the first and second gates and the first and second sources/drains; and

first and second contact plugs each in contact with the first gate and the second source/drain, respectively,

wherein the conductive patterns contact the upper surfaces of the first and second contact plugs.

3. The integrated circuit of Claim 1, wherein the conductive patterns are bit-line stud pads.

4. The integrated circuit of Claim 1, wherein the conductive patterns are disposed in a peripheral circuit domain of the semiconductor substrate.

5. The integrated circuit of Claim 1, wherein the thickness of the nitride film liner is from 100 Å to 1000 Å.

6. The integrated circuit of Claim 1, further comprising a metal interconnection in contact with the upper surface of the metal contact plug.

7. An integrated circuit comprising:

conductive patterns formed on a semiconductor substrate in first and second domains;

dielectric patterns disposed between the conductive patterns on the semiconductor substrate, each having a cross-section with an upside-down T shape and having a greater thickness than the conductive patterns;

a nitride film liner lining trenches defined by the conductive patterns and the dielectric patterns;

a dielectric layer in the second domain and filling the trenches;

nitride film studs having insubstantial step difference with respect to the dielectric patterns on the first domain, the nitride film studs covering the upper surfaces of the conductive patterns;

at least one capacitor in contact with a conductive region of the semiconductor substrate and passing through the dielectric patterns;

an intermetal dielectric layer on the capacitor and the dielectric layer; and

at least one metal contact plug in contact with at least one of the conductive patterns and passing through the intermetal dielectric layer, the dielectric layer and the nitride film liner.

8. The integrated circuit of Claim 7, wherein the first domain is a cell domain and the second domain is a peripheral circuit domain.

9. The integrated circuit of Claim 7, further comprising:

first and second gates and first and second sources/drains each formed in the second domain;

a plurality of third gates and a plurality of third sources/drains in the first domain;

a lower dielectric layer formed on the first, second and third gates and the first, second and third sources/drains;

first and second conductive pads formed within the lower dielectric layer and contacting a plurality of third source/drains; and

first, second and third contact plugs passing through the lower dielectric layer and in contact with upper surfaces of the first gate,

wherein the conductive pads contact the upper surfaces of the first, second and third contact plugs, and the conductive region includes the upper surface of the first conductive pad.

10. The integrated circuit of Claim 7, wherein the conductive patterns are bit line stud pads.

11. The integrated circuit of Claim 7, wherein the thickness of the nitride film liner is from 100 Å to 1000 Å.

12. The integrated circuit of Claim 7, further comprising a second dielectric layer formed on the nitride film studs, the dielectric patterns and the first dielectric layer, wherein at least one capacitor is formed to pass through the second dielectric layer, and wherein at least one metal contact plug passes through the second dielectric layer.

13. The integrated circuit of Claim 7, further comprising a metal interconnection in contact with the upper surface of the metal contact plug.

14. A method of fabricating an integrated circuit comprising the steps of:

forming conductive patterns on a semiconductor substrate;

forming dielectric patterns between the conductive patterns on the semiconductor substrate, each having a cross-section with an upside-down T shape and a thickness greater than the conductive patterns;

lining trenches defined by the conductive patterns and the dielectric patterns with a nitride film;

forming a dielectric layer on the nitride film to thereby fill the trenches; and

forming at least one metal contact plug passing through the dielectric layer and the nitride film liner and in contact with at least one of the conductive patterns.

15. The method of Claim 14, wherein the step of forming conductive patterns is preceded by:

forming first and second gates and first and second sources/drains on the semiconductor substrate;

forming a lower dielectric layer on the first and second gates and the first and second sources/drains; and

forming the first and second contact plug passing through the lower dielectric layer and in contact with the first gate and the second source/drain,

wherein the conductive patterns contact the upper surfaces of the first and second contact plugs.

16. The method of Claim 14, wherein the conductive patterns are formed in a peripheral domain of the semiconductor substrate.

17. The method of Claim 14:

wherein the step of forming the conductive patterns comprises the steps of:

sequentially forming a nitride film and a conductive film on the semiconductor substrate; and

forming conductive patterns and nitride patterns by patterning the conductive layer and the nitride film,

wherein the step of forming the dielectric patterns comprises:

forming a dielectric layer to have an insubstantial step difference with respect to the conductive patterns and the nitride patterns on the conductive patterns and the nitride patterns;

forming remnant nitride patterns by etching a predetermined thickness of each of the nitride patterns from the resultant having the dielectric layer; and

etching portions of the dielectric layer and the remnant nitride patterns.

18. The method of Claim 17, wherein the step of forming the dielectric layer comprises the steps of:

forming an dielectric layer filling gaps between the conductive patterns and the nitride patterns; and

performing chemical mechanical polishing (CMP) the upper surface of the dielectric layer to expose the nitride patterns.

19. The method of Claim 17, wherein the step of forming remnant nitride patterns is performed using an etching process in which the nitride patterns have etching selectivity with respect to the dielectric layer.

20. The method of Claims 17, wherein the step of etching portions of the dielectric layer and the remnant nitride patterns is performed using an etching process in which the remnant nitride patterns having insubstantial etching selectivity with respect to the dielectric layer.

21. The method of Claim 14, wherein the step of forming the conductive patterns comprises the steps of:

sequentially forming a conductive layer, an oxide film and a nitride film on the semiconductor substrate; and

forming conductive patterns, oxide film patterns and nitride patterns by patterning the conductive layer, the oxide film and the nitride film,

wherein the step of forming the dielectric patterns comprises the steps of:

forming a dielectric layer have an insubstantial step difference with respect to the conductive patterns, the oxide film pattern and the nitride patterns on the conductive patterns, the oxide film patterns and the nitride patterns;

etching the nitride patterns to expose the oxide film patterns; and

etching portions of the dielectric layer and the oxide film patterns.

22. The method of Claim 21, wherein the step of forming the dielectric layer comprises the steps of:

forming an dielectric layer filling gaps between the conductive patterns, the oxide film patterns and the nitride patterns; and

performing CMP on the upper surface of the dielectric layer to expose the nitride patterns.

23. The method of Claim 21, wherein the step of etching the nitride patterns is performed using an etching process in which the nitride patterns have etching selectivity with respect to the dielectric layer.

24. The method of Claim 21, wherein the step of etching portions of the dielectric layer and the oxide film patterns is performed using an etching process in which the oxide film patterns have insubstantial etching selectivity with respect to the dielectric layer.

25. The method of Claim 14, wherein the conductive patterns are bit line stud pads.

26. The method of Claim 14, wherein the thickness of the nitride film liner is from 100 Å to 1000 Å.

27. The method of Claim 14 further comprising the step of forming metal interconnections in contact with the upper surface of the metal contact plug, after the step of forming the metal contact plug.

28. A method of fabricating an integrated circuit, comprising the steps of:

forming conductive patterns on a semiconductor substrate in first and second domains;

forming dielectric patterns between the conductive patterns on the semiconductor substrate, each having a cross-section with an upside-down T shape and a thickness greater than the conductive patterns;

lining trenches defined by the conductive patterns and the dielectric patterns with a nitride film;

forming a dielectric layer that fills the lined trenches;

forming nitride film studs having insubstantial step difference with respect to the dielectric patterns, the nitride film studs covering upper surfaces of the conductive patterns;

forming at least one capacitor passing through the dielectric patterns to contact a conductive region of the semiconductor substrate;

forming a planarized intermetal dielectric layer on the capacitor; and

forming at least one metal contact plug passing through the dielectric layer and the nitride film liner to contact at least one of the conductive patterns.

29. The method of Claim 28, wherein the step of forming conductive patterns is preceded by:

forming first and second gates and first and second sources/drains, a plurality of third gates and a plurality of third sources/drains in the second domain and the first domain, respectively;

forming a lower dielectric layer on the first, second and third gates and first, second and third sources/drains;

forming first and second conductive pads to contact a plurality of third sources/drains within the lower dielectric layer; and

forming first, second and third contact plugs passing through the lower dielectric layer to contact upper surfaces of the first gate, the second source/drain and the second conductive pad,

wherein the conductive patterns contact the upper surfaces of the first, second and third contact plugs, and the conductive region is the upper surface of the first conductive pad.

30. The method of Claim 28, wherein the first domain is a cell domain, and the second domain is a peripheral circuit domain.

31. The method of Claim 28, wherein the step of forming conductive patterns comprises:

sequentially forming a conductive layer and a nitride film on the semiconductor substrate; and

forming conductive patterns and nitride patterns by patterning the conductive layer and the nitride film,

wherein the step of forming dielectric patterns comprises:

forming a dielectric layer having insubstantial step difference with respect to the conductive patterns and the nitride patterns on the conductive patterns and the nitride patterns;

forming remnant nitride patterns by etching a predetermined thickness of the nitride patterns; and

etching portions of the dielectric layer and the remnant nitride patterns.

32. The method of Claim 31, wherein the step of forming a dielectric layer comprises:

forming a dielectric layer filling gaps between the conductive patterns and the nitride patterns; and

performing CMP on the upper surface of the dielectric layer to expose the nitride patterns.

33. The method of Claim 31, wherein the step of forming remnant nitride patterns is performed using an etching process in which the nitride patterns have etching selectivity with respect to the dielectric layer.

34. The method of Claim 31, wherein the step of etching portions of the dielectric layer and the remnant nitride patterns is performed using an etching process in which the remnant nitride patterns have insubstantial etching selectivity with respect to the dielectric layer.

35. The method of Claim 28, wherein the step of forming the conductive patterns comprises:

sequentially forming a conductive layer, an oxide film and a nitride film on the semiconductor substrate; and

forming conductive patterns, oxide film patterns and nitride patterns by patterning the conductive layer, the oxide film and the nitride film;

wherein the step of forming the dielectric patterns comprises:

forming a dielectric layer having insubstantial step difference with respect to the conductive patterns, the oxide film patterns and the nitride patterns on the conductive patterns, the oxide film patterns and the nitride patterns;

etching the nitride patterns to expose the oxide film patterns; and

etching portions of the dielectric layer and the oxide film patterns.

36. The method of Claim 35, wherein forming a dielectric layer comprises:

forming an dielectric layer filling gaps between the conductive patterns, the oxide film patterns and the nitride patterns; and

performing CMP on the upper surface of the dielectric layer so that the nitride patterns are exposed.

37. The method of Claim 35, wherein the step of etching the nitride patterns is performed using an etching process in which the nitride patterns have etching selectivity with respect to the dielectric layer.

38. The method of Claim 35, wherein the step of etching a portion of the dielectric layer and the oxide film patterns is performed using an etching process in which the oxide film patterns have insubstantial etching selectivity with respect to the dielectric layer.

39. The method of Claim 28, wherein the step of forming nitride film studs comprises:

forming a photosensitive film pattern to expose only the first domain;

etching the dielectric layer using the photosensitive film pattern as a mask, so that the nitride film liner of the first domain is exposed;

removing the photosensitive film pattern;

depositing nitride to fill the trenches for which the nitride film is exposed; and

planarizing the deposited nitride to expose the dielectric patterns.

40. The method of Claim 39, wherein the step of planarizing is performed using an etch back process.

41. The method of Claim 39, wherein the step of planarizing is performed using a CMP process.

42. The method of Claim 39, wherein the conductive patterns are bit line stud pads.

43. The method of Claim 28 further comprising forming a second dielectric layer on the nitride film studs, wherein at least one capacitor is formed to pass through the still another dielectric layer and wherein at least one metal contact plug is formed to pass through the still another dielectric layer.

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44. The method of Claim 28 further comprising forming metal interconnections to contact the metal contact plug.